NANO LETTERS

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Wafer-Scale Atomic Layer-Deposited TeO_x/Te Heterostructure P-Type Thin-Film Transistors

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Cite This: https://doi.org/10.1021/acs.nanolett.4c02969 Read Online

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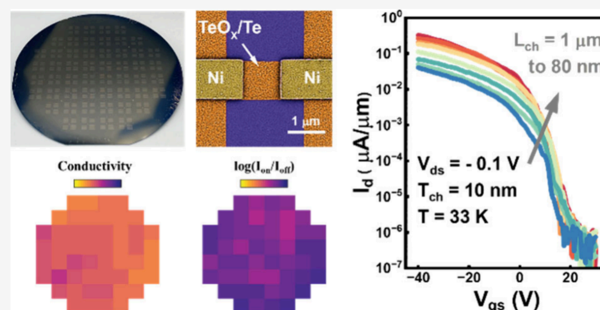
ABSTRACT: There is an increasing demand for p-type semiconductors with scalable growth, excellent device performance, and back-end-of-line (BEOL) compatibility. Recently, tellurium (Te) has emerged as a promising candidate due to its appealing electrical properties and potential low-temperature production. So far, nearly all of the scalable production and integration of Te with complementary metal oxide semiconductor (CMOS) technology have been based on physical vapor deposition. Here we demonstrate wafer-scale atomic layer-deposited (ALD) TeO_x/Te heterostructure thin-film transistors with high uniformity and integration compatibility. The wafer-scale uniformity of the film is evidenced by spatial Raman mappings and statistical electrical analysis. Furthermore, surface accumulation-induced good ohmic contact has been observed and explained by the unique band alignment of the charge neutrality level inside the Te valence band. These results demonstrate ALD TeO_x/Te as a promising p-type semiconductor for monolithic three-dimensional integration in BEOL CMOS applications incorporated with well-established n-type ALD oxide semiconductors.



KEYWORDS: *wafer scale, atomic layer deposition, negative Schottky barrier, tellurium oxide, tellurium, P-type thin-film transistor*

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As silicon semiconductor downscaling approaches quantum limits, there is an increasing demand for alternative materials to enable monolithic three-dimensional (M3D) integration, extending the semiconductor road map beyond current CMOS technology. The back-end-of-line (BEOL) M3D complementary metal oxide semiconductor (CMOS) constructions typically require processing temperatures below 300−400 °C to prevent degradation of front-end-of-line Si CMOS and interconnects, and flexible electronics demand even lower temperatures (below 200 °C).[1−3] Non-silicon n-type semiconductors, such as oxide semiconductors (e.g., In_2O_3 and IGZO)[4,5] and chalcogenides (e.g., MoS_2 and CdS),[6,7] are several candidates with good electrical performance and BEOL compatibility. While the scalable growth and performance of its p-type counterparts remain elusive and challenging, P-type oxide semiconductors are limited due to well-known oxygen 2p orbital-induced valence band (VB) edge localization.[8,9] Over the years, several candidates have emerged, such as transition metal dichalcogenides (e.g., WSe_2 and $MoTe_2$),[10,11] metal oxides (e.g., Cu_2O and SnO),[12−14] carbon nanotubes,[15,16] and organic semiconductors.[17] However, these materials either suffer from incompatibility with BEOL electronics or show poor stability and mobility. There is a need to identify alternative materials that can mitigate these issues and, at the same time, are compatible with existing CMOS platforms.

Recently, group VI tellurium (Te), a fascinating one-dimensional (1D) van der Waals (vdW) material, has attracted a great deal of interest owing to its high hole mobility, photoconductivity, thermoelectric characteristics, and spin-related physics.[18−22] Te has a chiral crystal structure with helical chains along the [0001] direction. Each 1D helical chain is bonded by the van der Waals interaction, arranged in hexagonal arrays (Figure 1a). From a device perspective, Te stands out as a promising p-type semiconductor for its high hole mobility, low processing temperature, and great air stability. So far, scalable and reliable production of Te is mainly based on physical vapor deposition techniques, including thermal evaporation, sputtering, molecular beam epitaxy, etc.[23−31] In terms of Te deposition based on atomic layer deposition (ALD), in 2019, Cheng et al. employed the ALD-Te recipe in the GeTe compound film,[32] while the uniformity is limited by isolated crystal islands. Recently, Kim et al. improved the ALD-Te recipe by introducing MeOH as a co-reactant and realized wafer-scale growth. Some electrical

Received: June 24, 2024
Revised: September 27, 2024
Accepted: September 27, 2024

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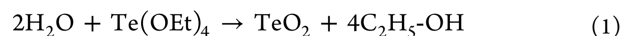
Figure 1. Characterization of ALD TeO_x/Te and materials. (a) Atomic structure of tellurium. (b) Optimized ALD-TeO_x process and ALD-Te process. (c and d) Representative Raman spectra of an annealed ALD-TeO_2 film and an as-grown ALD-Te film, respectively. (e) Photograph of 4 in. wafer-scale ALD TeO_x/Te films deposited on the SiO_2/Si substrate and XPS of the TeO_x/Te film. (f and g) Surface morphology of the as-grown TeO_x/Te thin film. The grain size is 50−100 nm with a surface roughness of 1.1 nm (RMS). (h) HAADF-STEM cross-section image and EDS mapping of a 20 nm thick ALD TeO_x/Te thin film. (i−k) HAADF-STEM image of random oriented crystallized Te domains.

functionalities have been shown on the basis of vertical p−n junctions.[33]

Here we demonstrate wafer-scale p-type field-effect transistors made from an ALD TeO_x/Te heterostructure. The thin layer of ALD-TeO_x serves as a connection between the oxide substrate and semiconducting Te, resulting in better coverage of the Te film (Figure S1). The TeO_x layer functions as not only a seeding layer but also a dielectric for the semiconducting Te due to its relatively large band gap of 3.2 eV.[34,35] Note that TeO_x in this work serves as the dielectric layer for a semiconducting Te channel instead of a p-type oxide semiconductor[29] because the as-grown TeO_x layer does not conduct electricity in our experiments. In ref 29, the authors demonstrated the design incorporating elemental Te within an amorphous TeO_x matrix. The structural characterizations and simulations given in ref 29 demonstrated that Te−Te bonds form and Te 5p states exist in an alloy-like Te-TeO_x film instead of a pure TeO_x layer. The as-deposited Te film exhibits good uniformity and isotropy along with promising electrical performance. The statistical analysis of the Raman shift and electrical performance over 500 devices across a 4 in. wafer is demonstrated. Because the charge neutrality level is aligned inside the valence band in Te, a negative Schottky barrier is observed in ALD-Te transistors, resulting in improved metal-to-semiconductor contacts. The total thermal budget for ALD TeO_x/Te is as low as 80 °C. These results demonstrate the potential of ALD-Te as a promising candidate for large-scale p-type semiconductor integration with BEOL compatibility.

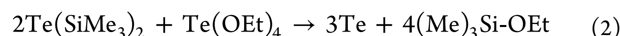
■ RESULTS AND DISCUSSION

ALD Growth of the TeO_x/Te Heterostructure. The ALD-TeO_x/Te growth involves two Te precursors: $Te(SiMe_3)_2$ (BTMS-Te) and $Te(OEt)_4$.[32,36,37] These two precursors enable the self-limited layer-by-layer growth of the heterostructure. We developed the ALD growth of TeO_x using the reaction of $Te(OEt)_4$ and H_2O:



$$2H_2O + Te(OEt)_4 \rightarrow TeO_2 + 4C_2H_5\text{-}OH \quad (1)$$

Semiconducting ALD-Te can be grown according to the following chemical reaction:



$$2Te(SiMe_3)_2 + Te(OEt)_4 \rightarrow 3Te + 4(Me)_3Si\text{-}OEt \quad (2)$$

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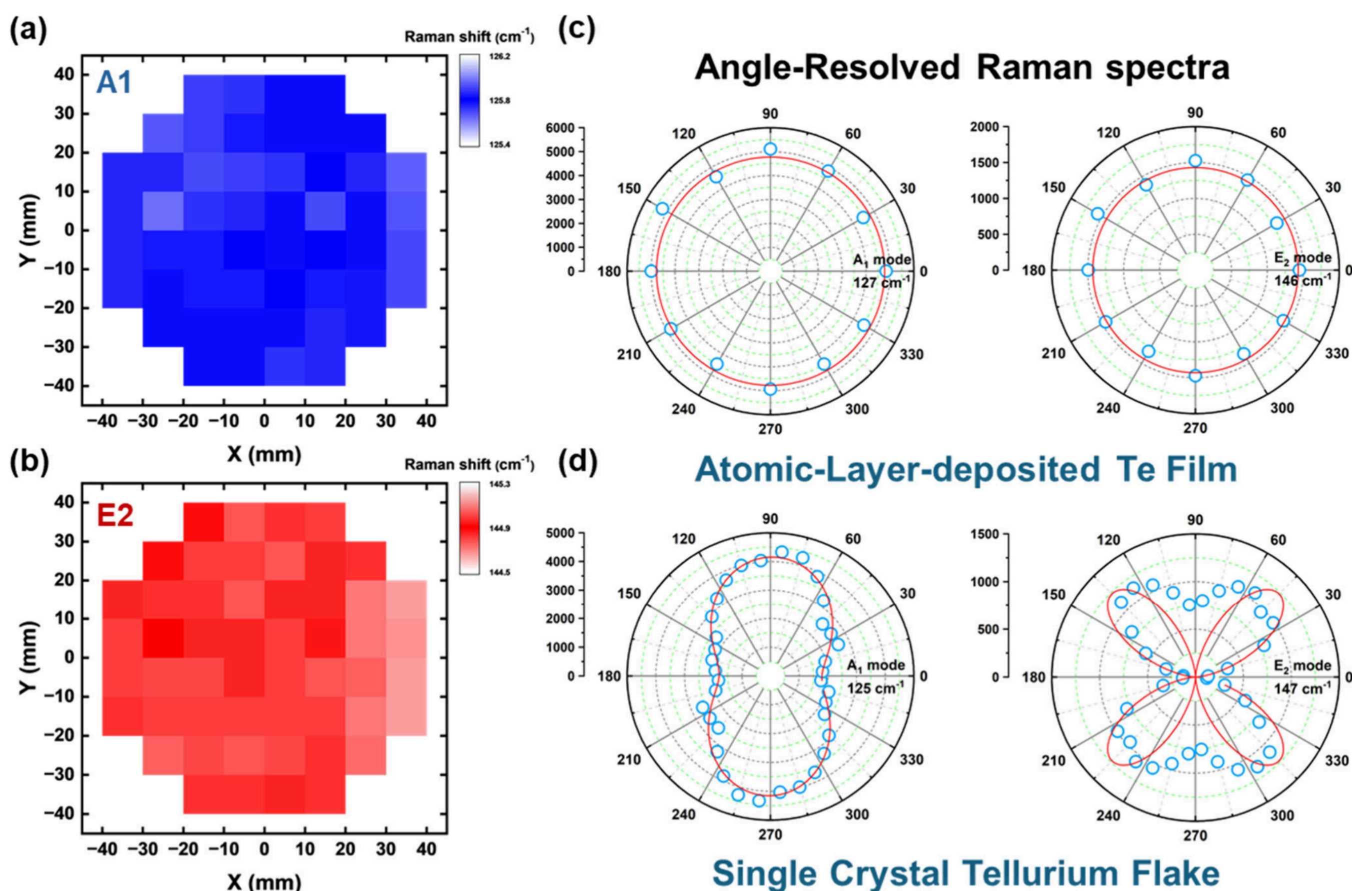
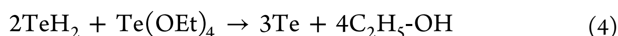


Figure 2. Spatial Raman spectral mapping and angle-resolved Raman spectra. (a and b) Spatial Raman spectral mapping for A_1 and E_2 modes over a 4 in. wafer. Each die has dimensions of 1 cm × 1 cm. (c and d) Polar figures of Raman intensity and fitting curves corresponding to A_1 and E_2 modes for ALD-Te and for a solution-grown Te single crystal.

In the experiment, MeOH is introduced as a co-reactant via a two-step reaction to improve the growth of ALD-Te by *in situ* formation of TeH_2. This process reduces the steric hindrance due to the smaller molecular volume and increases surface coverage:[33]

$$Te(SiMe_3)_2 + 2MeOH \rightarrow TeH_2 + 2MeOSiMe_3 \quad (3)$$



$$2TeH_2 + Te(OEt)_4 \rightarrow 3Te + 4C_2H_5\text{-}OH \quad (4)$$

A comparison of ALD-Te with and without MeOH dosing is shown in Figure S2.

Figure 1b shows the typical ALD-TeO_x process sequences. The ALD process was optimized at 80 °C. The as-grown TeO_x film is amorphous, but distinct Raman peaks of crystallized α-TeO_2 are observed in Figure 1c after annealing at 400 °C under an Ar atmosphere for 1 min. The semiconducting ALD-Te is then grown on top of the as-deposited amorphous ALD-TeO_x layer without annealing using the sequences shown in Figure 1b at 80 °C. Unlike ALD-TeO_x, the as-grown Te film is polycrystalline, with typical trigonal tellurium Raman peaks (Figure 1d). Three Raman-active modes located at 125 cm^{-1} (A_1 mode) and 145 cm^{-1} (E_2 mode) and split E_1 modes around 100 cm^{-1} were identified. The ALD-TeO_x layer connects the substrate oxide dielectric with the channel of semiconducting Te. The reaction between $Te(OEt)_4$ and water ensures the good nucleation of TeO_x and increases the rate of coverage of $Te(OEt)_4$ on the substrate, facilitating efficient reactions with the other precursor, BTMS-Te. This promotes the ALD growth of semiconducting Te. Using a customized ALD process (see Methods), a wafer-scale TeO_x/Te thin film was grown on 4 in. SiO_2/Si substrates. The rate of growth of ALD-TeO_x is ∼0.6 Å/cycle, and that of ALD-Te is ∼1.0 Å/cycle. The surface chemical composition of the TeO_x/Te film is analyzed by X-ray photoelectron spectroscopy (XPS) (Figure 1e and Figure S3). Neutral Te^0 (from Te) dominates, and Te^{4+} (from TeO_2) is also present in the film. The surface morphology of the film was characterized by scanning electron microscopy (SEM) and atomic force microscopy (AFM), as shown in panels f and g, respectively, of Figure 1. The average grain size is 50−100 nm, and the surface roughness is <1.1 nm (RMS). The structure and composition of the ALD-Te films were analyzed by high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) and energy-dispersive X-ray spectroscopy (EDS) (see Methods). Figure 1h shows the cross-sectional STEM image and EDS mapping of the as-grown Te thin film, clearly depicting a continuous Te film with a thickness of 20 nm. Notably, random oriented atomic chains were observed in different crystallized Te domains, as shown in Figure 1i−k. A hexagonal lattice structure is observed in Figure 1i, while tilted helical chains along the [0001] direction are visible in panels j and k of Figure 1. These random orientations contribute to the isotropic properties of the ALD-Te film.

The wafer-scale uniformity and isotropy of the ALD-Te films were characterized by spatial Raman spectral mapping, angle-resolved Raman spectra, and angle-dependent electrical

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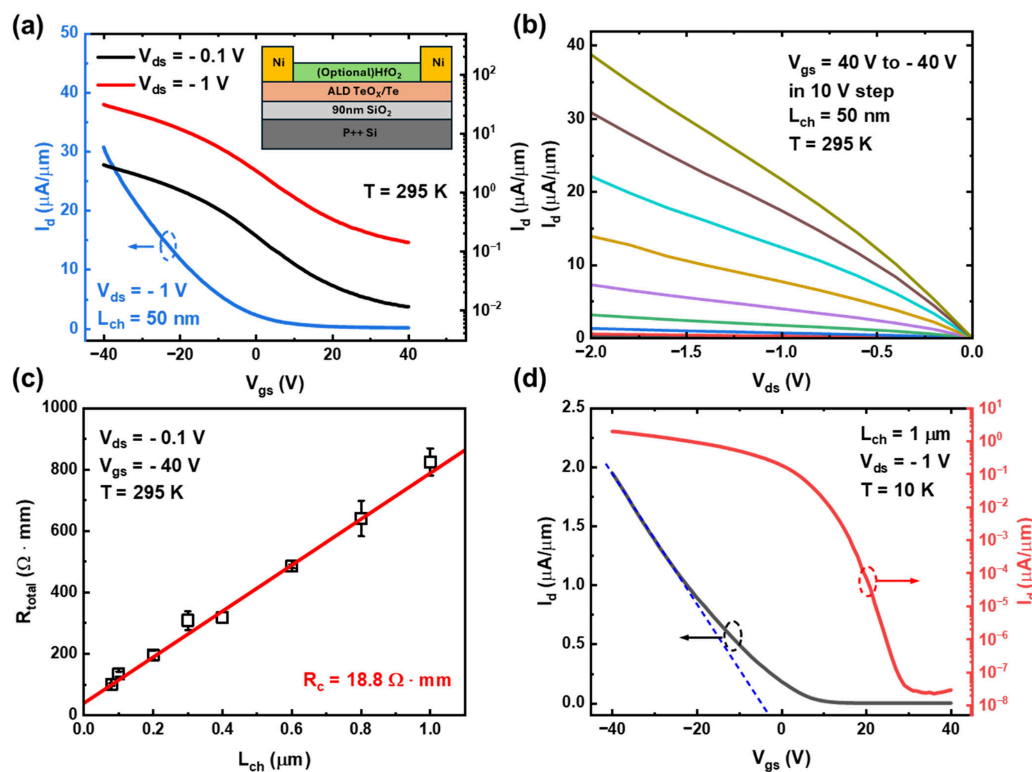

Figure 3. Electrical performance of ALD TeO_x/Te field-effect transistors. (a) Transfer characteristic of a typical short channel ALD TeO_x/Te FET with an L_{ch} of 50 nm measured at room temperature. The total thickness of ALD TeO_x/Te is 10 nm. The channel width is 1 μm. The inset shows the schematic of the device structure. The gate bias sweeps from positive to negative. (b) Output characteristic of the same short channel device. (c) Transfer length method measurements of the 10 nm thick ALD TeO_x/Te FETs. Each data point is averaged by at least five devices. (d) Transfer characteristic of a long channel (L_{ch} = 1 μm) device with the same channel thickness measured at 10 K.

resistance at room temperature. Panels a and b of Figure 2 show the spatial Raman spectral mappings for tellurium A_1 and E_2 modes on a 4 in. wafer. The good homogeneity and uniformity are verified by the variation of the peak position of the A_1 and E_2 modes being <0.3%. Angle-dependent Raman spectra of ALD-Te compared to those of a single-crystal Te flake are shown in panels c and d, respectively, of Figure 2. Upon rotation of the single-crystal tellurium flake in steps of 10°, changes in the angle-resolved Raman peak intensities were clearly identified and plotted in polar figures, agreeing with previous results.[18,38] These strong angle-dependent optical responses are due to the intrinsic structural anisotropy, while for ALD-Te, the radial plot of the Raman mode intensity as a function of sample angle is angle-invariant, suggesting that the ALD-Te film is isotropic. Further experiments involving angle-dependent electrical resistance were conducted on ALD-Te, as shown in Figure S4. Twelve radial Ni electrodes were fabricated at intervals of 30°, and the electrical resistance across the sample was measured in different directions. The angle-invariant radial plot of the electrical resistance confirms the electrical isotropy of the ALD-Te films, which provides possibilities for large-scale electronics application and integration.

Device Characterization of ALD TeO_x/Te Thin-Film Transistors. To explore the potential of ALD TeO_x/Te toward nanoelectronics applications, we investigated the electrical performance of ALD TeO_x/Te field-effect transistors (FETs). The low growth temperature of 80 °C makes it a promising candidate for a BEOL compatible p-type semiconductor. Back-gate top contact FETs were fabricated on ALD TeO_x/Te with different thicknesses and channel lengths. The device structure, including an optional HfO_2 passivation layer, is illustrated in Figure 3a. The typical transfer (Figure 3a) and output (Figure 3b) characteristics of 50 nm channel length, 10 nm thick ALD TeO_x/Te FETs show a decent on/off ratio approaching 10^3 at room temperature due to a narrow band gap of 0.35 eV for bulk Te. The transfer characteristics of ALD TeO_x/Te thin-film transistors (TFTs) with different thicknesses are shown in Figure S5. The on/off ratio increases as the thickness decreases from 16 to 10 nm. The significant improvement of the on/off ratio is expected to be in the <5 nm region due to the quantum confinement effect. Te has significant quantum capacitance due to its high electron and hole mobility. A higher on/off ratio could be achieved by reducing film thicknesses[18] or measurement temperatures that will be discussed below. The linear output characteristic demonstrates good ohmic contact. An on current of 39 μA/μm is achieved at a V_{ds} of −2 V and a V_{gs} of −40 V. Figure 3c shows the channel length scaling of the ALD TeO_x/Te transistors. Using the transfer length method (TLM), a relatively low contact resistance of 18.8 Ω mm for p-type channels is observed. The gate-dependent contact resistance and sheet resistance are shown in Figure S6. The decreases in R_c and R_{sh} at a lower gate bias are due to a higher carrier concentration in the channel and contact region induced by the field effect. Tellurium has a narrow band gap of 0.35 eV, making device performance strongly dependent on temperature due to the low thermal activation of carriers. Figure 3d shows the low-temperature device performance of the ALD TeO_x/Te FETs. The device operates in enhancement mode

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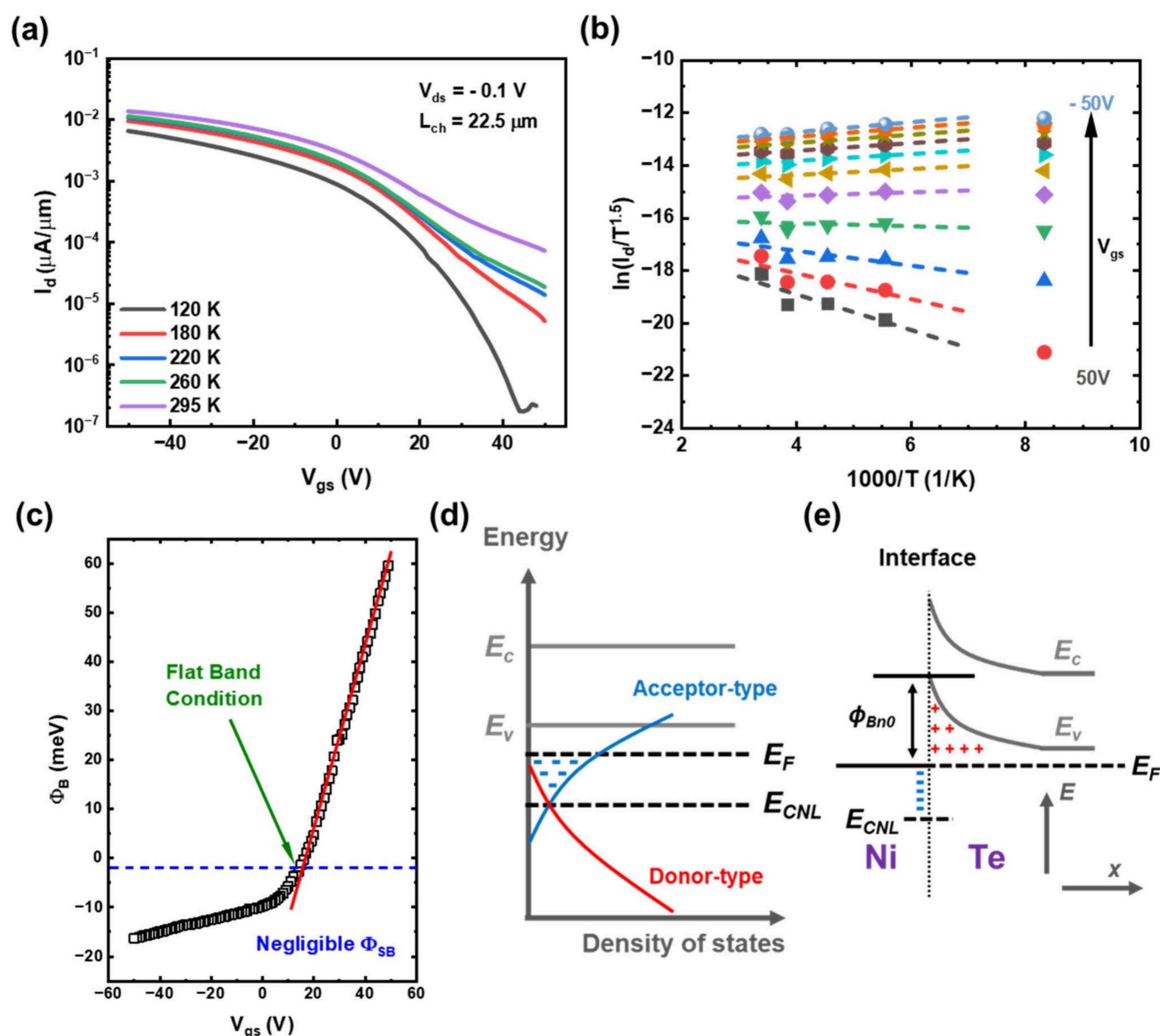

Figure 4. Negative Schottky barrier at the Ni/Te contact. (a) Temperature-dependent transfer characteristics of a 14 nm thick long channel device. (b) Arrhenius plot at different gate biases extracted from the temperature-dependent transfer curves. (c) Extracted gate-dependent contact barrier height from the Arrhenius plot. A negative Schottky barrier is observed under the flat band condition. (d and e) Schematic of the trap density at the Te interface and band alignment with Ni contact, respectively.

with an on/off ratio of >10^8 at 10 K. The field-effect mobility decreases with temperature (Figure S7), indicating a grain boundary-dominated electrical transport mechanism.[31]

The device performance of a two-dimensional Schottky FET is typically dominated by the high Schottky barrier (high contact resistance) at the metal−semiconductor junction[39−44] due to the effect of Fermi level pinning. Achieving a good ohmic contact on p-type transistors is particularly challenging.[39−42] The negative Schottky barrier is achieved in ALD-InO_x n-type thin-film transistors with enhanced device performances,[45,46] where the charge neutrality level (CNL) is aligned inside of the conduction band. In tellurium, there is a p-type accumulation layer related to surface native oxide.[47,48] At the Te surface, the CNL is aligned inside the valence band, providing extra charges in the contact region. This can result in surface accumulation and a negligible Schottky barrier. In experiments, the Schottky barrier can be extracted using the equation $I_{ds} = A^*T^{1.5}\exp(-\Phi_B/k_BT)$, where A^* is the Richardson constant and k_B is the Boltzmann constant. Figure 4a shows the temperature-dependent transfer characteristics of a 14 nm thick ALD TeO_x/Te FET. By plotting $\ln\left(\frac{I_{ds}}{T^{1.5}}\right)$ versus $1000/T$ at different gate voltages, as shown in Figure 4b, we calculated the gate-dependent barrier height (Figure 4c). The Schottky barrier is extracted to be negative under the flat band condition. It is worth mentioning that barrier height extraction is no longer accurate when the barrier height is negative because the formula is based on the thermal activation of electrons (holes) over a positive barrier. However, the extremely small Schottky barrier height indicates the origin of good ohmic contact. The contact resistance is not extremely low, potentially related to the doping concentration and a low surface coverage-induced resistant network. Figure 4d shows the schematic energy alignment of the Fermi level (E_F), valence band edge (E_v), and charge neutrality level (E_{CNL}) in tellurium. At the metal−semiconductor interface, the negatively charged acceptor-type traps attract positive charges inside of tellurium, causing the band bending (negative Schottky barrier) indicated in Figure 4e.

Devices with channel lengths ranging from 4 to 25 μm, fabricated on a 4 in. wafer-scale ALD TeO_x/Te thin film, were measured and analyzed to evaluate their electrical performance and uniformity. Figure 5a illustrates the transfer characteristics of two different channel lengths at room temperature within a

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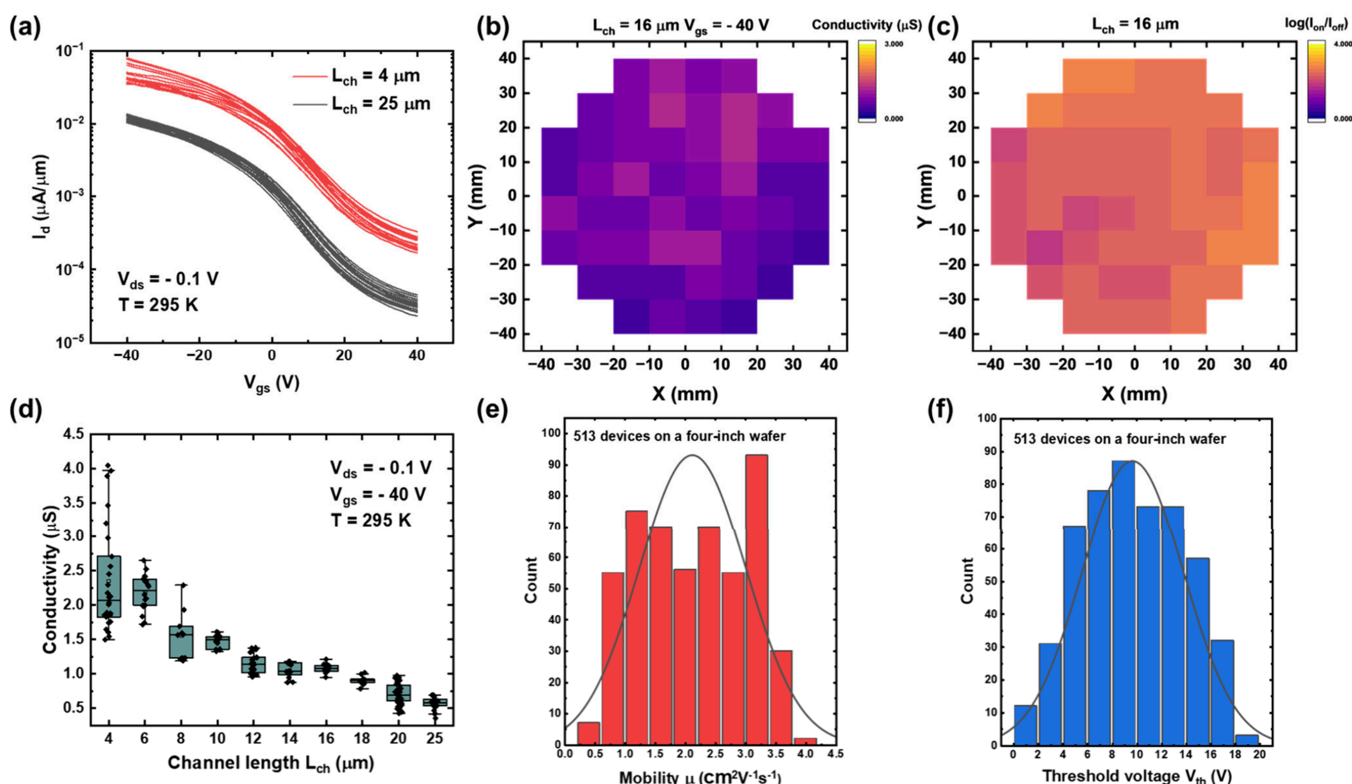

Figure 5. Wafer-scale electrical conformity of the ALD TeO_x/Te film. (a) Statistical electrical performance of two different channel length ALD TeO_x/Te FETs (L_{ch} = 25 and 4 μm) at room temperature. (b and c) Spatial color mapping of conductivity and on/off ratio, respectively, over a 4 in. wafer. Each die has dimensions of 1 cm × 1 cm. (d) Statistical analysis of the channel length scaling. (e and f) Histograms of field-effect mobility and threshold voltage, respectively, obtained from 513 devices with an L_{ch} of 16 μm.

single die. The devices with long channels exhibit less variation in performance due to the averaging effect of grain boundaries. By averaging the results from at least 10 devices within each die, we generated color maps of conductivity at a V_{gs} of −40 V and the on/off ratio across the entire 4 in. wafer, as shown in panels b and c of Figure 5. These color maps reveal that the conductivity is relatively low at the wafer edges, indicating thickness variations in marginal regions due to the limitation of the ALD chamber. Despite this, the on/off ratio remains consistent, ∼3 orders of magnitude across the entire wafer with minimal variations, underscoring the uniformity of the ALD process. The channel length scaling of conductivity within one die is plotted in Figure 5d, providing insight into the device behavior under varying channel dimensions. Panels e and f of Figure 5 present histograms of the field-effect mobility and threshold voltage, respectively, obtained from 513 devices with a channel length of 16 μm, showing an average field-effect mobility of 2.5 $cm^2 V^{-1} s^{-1}$. The relatively high uniformity and reproducibility of these devices across a large wafer are promising for large-scale production.

■ CONCLUSION

In summary, we achieved BEOL compatible wafer-scale ALD growth of TeO_x/Te films for p-type field-effect transistors, demonstrating good uniformity, conformity, and isotropy based on material characteristics and statistical analysis of devices over a 4 in. wafer. Furthermore, the low contact resistance enabled by the negative Schottky barrier ensures efficient carrier injection, which is particularly beneficial for p-type transistors. Our comprehensive analysis demonstrates that ALD TeO_x/Te is a viable p-type semiconducting material for wafer-scale integration. The ability to fabricate devices with consistent performance over a large area supports their potential for use in advanced CMOS technology and other electronic applications with wafer scalability. This work highlights the advantages of using ALD techniques to achieve high-quality semiconductor channels beyond the dielectrics.

■ METHODS

Atomic Layer Deposition of Te and TeO_x. A TeO_x thin film was deposited in a 4 in. compatible ALD chamber. $Te(OEt)_4$ and H_2O were used as precursors. The ALD pedestal temperature was set to 80 °C, and the chamber pressure was stabilized at 500 mTorr during the deposition. $Te(OEt)_4$ was heated at 65 °C, and the water was kept at room temperature. The precursors were delivered to the chamber with a 20 sccm Ar carrier gas. The as-deposited TeO_x film looks blueish under an optical microscope.

The Te film was deposited using $Te(SiMe_3)_2$ (BTMS-Te) and $Te(OEt)_4$ as Te precursors, while MeOH was introduced as a co-reactant to provide *in situ* precursor TeH_2. The vapor pressures of BTMS-Te, $Te(OEt)_4$, and MeOH are 1 Torr (at 25 °C), 1 Torr (at 85 °C), and 127.2 Torr (at 25 °C), respectively. The ALD pedestal temperature was set to 80 °C, and the chamber pressure was stabilized at 500 mTorr during Ar purge and 5000 mTorr during the Te deposition due to the high vapor pressure of MeOH. The BTMS-Te and $Te(OEt)_4$ contained in the bubbler were heated at 35 and 65 °C, respectively, and delivered to the chamber with 20 sccm Ar carrier gas. The MeOH bubbler was maintained at room temperature, and its injection was also aided by 20 sccm Ar carrier gas. The flow rate for Ar purging was 100 sccm. The

https://doi.org/10.1021/acs.nanolett.4c02969
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typical ALD sequence of one cycle involving methanol dosing and a discrete feeding method is typically as follows. Three pulses of MeOH (500 ms) overlapped with BTMS-Te (2 s) divided by a 10 s Ar purge, followed by three pulses of $Te(OEt)_4$ (2 s) divided by a 10 s Ar purge. The as-deposited Te film looks yellowish with metallic luster under an optical microscope.

Raman Spectra and Structural Characterization. Angle-resolved Raman spectra with a He−Ne excitation laser with a wavelength of 633 nm were measured at room temperature. The dimension of the laser spot was 1 μm. The system was calibrated with the Raman peak of Si at 520 cm^{-1} before measurement. The incident light entered perpendicular to the Te flake and was polarized parallel to the spiral atom chains or long axis of single-crystal Te. A linear polarizer was placed in front of the spectrometer to polarize reflected light in the same direction as incident light. By rotating the Te flake in steps of 10°, we observed an angle-resolved Raman peak intensity change. The peak intensities of different modes were fitted with a Lorentz function and plotted as polar figures. These results were then fitted by multiplying the corresponding Raman tensors. The same measurement was conducted on ALD-Te with a similar thickness. The peak positions slightly deviate from that of single-crystal Te due to the difference in thickness, while no angular dependence was observed, which confirms the isotropic nature of the ALD-Te films.

The surface morphology and thickness of the ALD Te film were analyzed by atomic force microscopy (Park AFM). High-resolution RTEM was performed with an FEI Talos F200x system equipped with a probe corrector operated at 200 kV, and EDS data were collected by an X-MaxN100TLE detector. HAADF imaging was performed using a JEOL dark-field detector with a high-angle tilt holder. XPS was conducted with a Kratos Axis Ultra DLD instrument.

FET Device Fabrication and Characterization. Bottom-gate top contact FETs were fabricated on 90 nm SiO_2/p^+Si. After solvent cleaning and low-power oxygen plasma treatment of the SiO_2/p^+Si substrate, ALD of TeO_x/Te was performed at 80 °C, using BTMS-Te and $Te(OEt)_4$ as Te precursors. A wide range of distances between the source and drain electrodes are defined in the masks so that both short and long channel lengths can be achieved. Then, ICP dry etching using BCl_3/Ar plasma was used to accurately define the channel width. The 50/50 nm Ni/Au metal contacts were deposited by e beam evaporation. We chose Ni/Au as the contact metal because Ni has a relatively high work function that reduces the Schottky contact barrier and can sustain relatively high temperatures. A 5 nm HfO_2 optional passivation layer was deposited by ALD at 120 °C with $[(CH_3)_2N]_4Hf$ and H_2O as the Hf and O precursors, respectively.

Electrical characterization was carried out with a Keysight B1500 system and a Cascade Summit probe station in N_2 environments at room temperature. Temperature-dependent electrical measurements were performed in a LakeShore cryogenic probe station at high vacuum with a Keysight B1500 system. The field effective mobility was calculated using the formula $\mu_{FE} = g_m L/W C_{OX} V_{DS}$, where g_m, L, W, and C_{OX} are the transconductance, channel length, channel width, and gate oxide capacitance, respectively. The threshold voltage is extracted by a constant current method with a cutoff current of 1 nA. For isotropic transport measurements, the as-deposited ALD Te films were first patterned with EBL and dry etched into a round shape. Then, 12 Ni electrodes were patterned and deposited with 30° offset in sequence.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.4c02969.

Additional data and details for the effect of methanol dosing in ALD-Te, angle-dependent resistance, transmission line methods extracting contact resistance, sheet resistance for ALD TeO_x/Te, and temperature-dependent electrical performance, and supporting notes 1−4 (PDF)

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Author Contributions

P.T. and C.N. contributed equally to this work. P.D.Y. conceived and supervised the project. P.T., C.N., and Z.L. designed the experiments. The precursors are supported by G.W. from ASM. P.T. and Z.L. set up the precursors for ALD.

P.T. synthesized the material and fabricated the devices. P.T. and C.N. performed the measurements. P.T., C.N., J.-Y.L., and L.L. analyzed the data. Y.Z. performed TEM under the supervision of H.W. P.T. and C.N. wrote the manuscript, and all of the authors commented on it.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

ALD of TeO_x/Te was partly supported by ASM and partly supported by National Science Foundation Grant CMMI-2046936. P.T. acknowledges technical support from Dmitry Y. Zemlyanov.

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https://doi.org/10.1021/acs.nanolett.4c02969
Nano Lett. XXXX, XXX, XXX−XXX